REMARKS / ARGUMENTS

Applicant thanks the Examiner for the courtesy extended to the Applicant's agent in the telephone interview on 19 April 2007. That interview covered:

1. The relationship between Yamanaka et al. and claim 1. Applicant's agent pointed out that Yamanaka, as understood, fails to disclose the "broadcasting" feature as recited in claim 1. Yamanaka only adjusts a slave clock which the Examiner has equated with the time of the second bus - adjusting the time of the second bus itself is not the same as adjusting timing of a device on the second bus.
2. The appropriateness of amendment to specify "midway" in claim 2 and the disclosure. To a person skilled in the art (e.g. a computer hardware/software designer) it is obvious that the time measurement of the second bus must be taken midway (i.e. half-way) between the two time measurements of the first bus for the example described in paragraph [0016] to work. The Examiner has pointed this out. MPEP 2163.07 states that "By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter."

Pending Claims

Claims 1, 3-12, 13, 15 to 17, 19 to 20, 22 to 32 are pending after this amendment. Claims 2, 12 and 18 have been cancelled to simplify issues in this application. Other claims have been amended to more clearly delineate the claimed invention.

Compliance with 35 U.S.C. §102 and §103

The Office Action alleges that all of the features in the previously-pending independent claims are disclosed by U.S. Patent No. 4,807,259 (Yamanaka). The Applicant submits that this is incorrect. Claim 1 , as amended, expressly recites that:

- the first bus is associated with a first clock that generates first bus timing information for the first bus;
- the second bus is associated with a second clock that generates second bus timing information for the second bus; and,
- each of the devices has an individually adjustable timing.

As understood, Yamanaka *et al.* disclose sending encoded timing signals between a master station and a slave station in order to synchronize the time of a slave clock in the slave station with the time of a master clock in the master station. The master station and slave stations each have an internal bus. The master station exerts centralized control over a data link between the master and slave station (see col. 1, ln. 41-43) and synchronizes the slave clocks with the master clock by exchanging messages with the slave stations. Synchronization is performed separately for each slave station. The slave station uses the slave clock time directly.

Claims 1 to 11, 13, 15 to 17 and 30

As discussed with the Examiner, claim 1 recites at least four entities that maintain timing, namely, the first and second buses, one or more devices on the first bus, and one or more devices on the second bus. Yamanaka *et al.* fails to provide this context.

If: the first and second buses claimed in claim 1 are equated with the buses (51, 52) in the master and slave stations, and the timing information from the first bus and the second bus in claim 1 is equated with the times (TM, TS) maintained by the master and slave clocks (17, 27); then there is nothing in Yamanaka to equate with the claimed devices which each have individually-adjustable timing. Yamanaka, as understood fails to disclose any devices on the first or second buses that maintain adjustable timing information independently of master clock (17) or slave clock (27). The time TS of Yamanaka's slave clock (27) cannot be both timing information of the second bus and timing of a device on the second bus, as alleged.

Further, Yamanaka fails to disclose "broadcasting the timing offset to the one or more devices on the second bus so that the one or more devices on the second bus can adjust their timing to be synchronized with the one or more devices on the first bus" as recited in claim 1. This is not necessary in the Yamanaka system because any components in the slave station can use (TS), the timing of the slave clock (27,37) to decide when to take certain actions. Slave clock (27,37) is kept synchronized with the master clock (17) to a desired degree of accuracy.

Therefore, it is submitted that independent claim 1 patentably distinguishes Yamanaka *et al.*

The Applicant respectfully requests rejoinder of claims 5, 8, 10, 11 and 13 on the basis that allowable claim 1 is generic to all of claims 3 to 11, 13 and 15 to 17 and also claim 5 has been amended to depend from claim 4.

The Applicant submits that dependent claims 3 to11, 13, 15 to 17, and 30 which all depend from claim 1, are patentable over Yamanaka *et al.* at least because they depend from claim 1.

Claims 3 to 5

In relation to claims 3 to 5, the Applicant submits that Baker fails to remedy the defects of Yamanaka or to disclose the features claimed in claims 4 and 5. Baker, as understood, discloses methods for measuring PCR jitter, frequency offset and drift rate in received MPEG video signals. The cited portions of Baker do not disclose broadcasting a drift rate of a timing offset as claimed in claims 3 to 5. The drift rate described by Baker is a drift rate of a frequency (see Baker col. 4, ln. 4). Further Baker's purpose is to measure characteristics of the MPEG video signal such as the frequency drift rate. Baker, as understood, does not broadcast measured drift rates to any device to permit the device to adjust its timing. Further, Baker's techniques do not appear to be applicable in the context of Yamanaka (since Baker apparently requires decoded PCR values from an encoded MPEG transport stream and PCR intervals to operate - see col. 4ll. 10-14 - and Yamanaka does not provide these values).

Claim 9

Claim 9 recites "the cameras adjust their timing by selectively reading an adjustable amount of extra data from a light-sensing array for each frame". The Examiner has cited Pennywitt for this feature. The cited portion of Pennywitt, as understood, discloses adding extra data bytes to a frame in a framer in order to synchronize data rates of transmitted data. This is not equivalent to reading an adjustable amount of extra data for a frame within a video camera. Pennywitt is discussing frames in the data-transmission context. In claim 9, "frame" relates to a video frame (see e.g. para [0034]).

Claim 30

Claim 30 recites "simultaneously broadcasting the timing offset to a plurality of devices on the second bus and individually regulating a timing of each of the plurality of devices on the second bus based at least in part upon the timing offset". The Examiner has indicated that it would be obvious to combine Yamanaka with Chaudhry to provide this feature in the context of claim 1. The Applicant submits that this is incorrect. Chaudhry discloses a multi-processor system in which redundant processors work in lock step. Chaudhry's processors do not have individually-variable timing as claimed in claim 1.

Claims 19 to20 and 31

The Applicant reiterates out that independent claim 19 recites at least five entities that maintain timing, namely, the first, second and master buses, one or more devices on the first bus, and one or more devices on the second bus.

The Office Action apparently asserts the following correspondence between features of Yamanaka and claim 19:

Yamanaka	Claim 19
bus (51)	master bus
bus (52)	first bus
bus (53)	second bus
TM	time of master bus
TS (of slave clock (27))	time of first bus
TS (of slave clock (37))	time of second bus

The Applicant points out that Yamanaka fails to disclose any devices to which offset information is broadcast. The values TS maintained by slave clocks (27 and 37) cannot be equated to both timing information for their respective buses (52, 53) and timing of devices on the buses. Claim 19 recites "adjusting the timing of the one or more devices on the first bus based upon the first timing offset and the first bus timing information and adjusting the timing of the one or more devices on the second bus based upon the second timing offset and the second bus timing information so that the one or more devices on the first bus and the one or more devices on the second bus all begin their respective operational cycles at the same global time". This feature is not disclosed by Yamanaka.

The Applicant submits that the cited combination of Yamanaka and Chaudhry fails to render claim 31 non-compliant with 35 U.S.C. §103 for the same reasons as stated above in relation to claim 30.

Claims 22 to 29 and 32

Independent claim 22, as amended, recites "a timing control system in each of the one or more devices on the second bus, the timing control systems each configured to adjust a timing of a corresponding one of the devices based upon the second bus timing information and the timing offset". The claimed timing control system and devices are in addition to the first and second clocks. Applicant submits that these features are not disclosed by Yamanaka, as understood. As noted above, if the Yamanaka slave clocks (27, 37) are equated with the first and

second clocks then Yamanaka does not have a timing control system that adjusts timing of a device on buses (51, 52). Slave clocks (27, 37) cannot be both the claimed second clocks and the claimed devices. Therefore, claim 22 is submitted to distinguish Yamanaka et al.

Claim 29

In relation to claim 29, Applicant points out that if a person attempted to combine Yamanaka and Yagita then the person would either attempt to treat each camera as a slave station and synchronize each slave station as described by Yamanaka or provide a slave clock accessible to all of the cameras and keep the slave clock synchronized with a master clock as described by Yamanaka. One would not arrive at the claimed invention which involves broadcasting the timing offset to the plurality of cameras.

The Applicant submits that the cited combination of Yamanaka and Chaudhry fails to render claim 32 non-compliant with 35 U.S.C. §103 for the same reasons as stated above in relation to claim 30.

The Applicant respectfully requests rejoinder of claims 27 and 28 on the basis that allowable claim 22 is generic to all of claims 23 to 29.

The Applicant accordingly submits that claims 22 to 29 and 32 are patentable over the cited references.

Conclusion

The Applicant submits that all pending claims of this application are in condition for allowance.

The Applicant respectfully requests reconsideration and allowance of this application.

Respectfully submitted,

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